USC Viterbi School of Engineering
Ming Hsieh Department of Electrical Engineering

Ming Hsieh Institute Seminar Series
Ming Hsieh Department of Electrical Engineering

Integrated Systems

Widely Tunable Active True-Time-Delay Line and Millimeter-Wave VCO

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Date: Tuesday, October 15th, 2019 - Time: 2:00pm - Location: EEB 132

Abstract: An all-pass filter architecture that can be generalized to high orders, and can be realized using active circuits is proposed. Using this, a compact true-time-delay element with a widely tunable delay and a large delay-bandwidth product is demonstrated. Coarse tuning of delay is realized by changing the filter's order while keeping the bandwidth constant and fine tuning is implemented by changing the filter's bandwidth utilizing the delay-bandwidth tradeoff. A test chip fabricated in 130nm CMOS process demonstrates a delay tuning range of 0.25 to 1.7ns over a bandwidth of 2GHz, while maintaining a magnitude deviation of +/-0.7 dB. The filter has a worst case noise figure of 23dB, and -40dB IM3 distortion for 37 mV ppd inputs. The chip dissipates 112 to 364 mW of power between its minimum and maximum delay settings. The filter's delay-bandwidth product of 3.4, which, combined with a small active area of 0.6mm^2, corresponds to a substantial improvement over the state-of-the-art of on-chip active delay lines.

A widely tunable millimeter wave quadrature VCO using two resonant modes in a resonator with a new 8-port coupled inductor structure is proposed. The structure is symmetric, uses single-turn coils, has short interconnections to active circuitry and avoids additional losses in the mode-switching circuitry. A prototype in 65nm LP bulk CMOS process tunes from 25GHz to 38GHz while consuming 17.5mW to 21.6mW from a 0.65V supply. The phase noise at 3MHz offset is -121 dBc/Hz at 25GHz and -111 dBc/Hz at 38GHz. At 3MHz offset, the measured figure of merit (FoM) and the tuning-range-FoM (FoMT) are in the range of 180-187 dB and 191-199 dB respectively.

Biography:

Dr. Nagendra Krishnapura obtained his BTech from the Indian Institute of Technology, Madras, India and his PhD from Columbia University, New York. He has worked as an analog design engineer at Celight, Multilink, and Vitesse semiconductor. He has taught analog circuit design courses at Columbia University as an adjunct faculty. He is currently a professor at the Indian Institute of Technology, Madras. His interests are analog and RF circuit design and analog signal processing.

Hosted by Prof. Hossein Hashemi, Prof. Mike Chen, Prof. Dina El-Damak, Prof. Manuel Monge, Prof. Constantine Sideris, and Prof. Mahta Moghaddam.
Organized and hosted by Aoyang Zhang (aoyangzh@usc.edu).